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10/792,115	03/02/2004	Phillip M. Sher	A1WI2176US	3931	
23935 MODDEL DA 3				EXAMINER	
KOPPEL, PATRICK & HEYBL 555 ST. CHARLES DRIVE			BURD, KEVIN MICHAEL		
SUITE 107 THOUSAND OAKS, CA 91360			ART UNIT	PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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n M. Burd	2611
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OF THIS COMMUNIC on no event, however, may a re- and will expire SIX (6) MONT	ply be timely filed THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).
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Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 1. Claims 1-4, 8-12, 34-38, 42-45 and 54 are rejected under 35 U.S.C. 102(e) as being anticipated by Fague et al (US 2004/0146122).

The applied reference has a common assignee and a number of common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 3, 4, 8, 12, 42 and 43, Fague discloses the radio frequency receiver shown in figure 1. The receiver comprises an analog gain control section for controlling the gain of a received RF signal. The programmable gain amplifiers 23 are controlled by the RSSI circuit 24 (paragraph 0024). The RSSI circuit 24 will recognize the presence of a data packet within the RF signal. This packet will be output from the

filter 22 and the RSSI circuit will ensure a constant signal is input to the AGC 26. The RSSI control loop comprises the "analog GO circuit". The receiver comprises a digital demodulator 32 for demodulating the output of the gain control section. The receiver comprises a preamble detect circuit 36 that recognizes the presence of a data packet within the received RF signal. The digital demodulator is shown in figure 2. The preamble detect circuit will enable components of the FO determination section 59 of figure 3 (paragraph 0032). The preamble detect circuit 36 is the "digital GO circuit". Control circuitry will be found in the RSSI control loop and the preamble detect circuits to enable the circuitry to function properly.

Regarding claim 2, the control circuitry enables the digital demodulator to output the proper compensated signal as described above.

Regarding claims 9, 44 and 45, the preamble is detected and is distinguished from the interference present in the signal. When no co-channel interference is present in the signal, the preamble is not distinguished from the co-channel interference.

Regarding claim 10, the preamble detect circuit 36 receives a FIR filtered signal (figure 1).

Regarding claim 11, the analog gain control section comprises the AGC 23, RSSI 24, ADC 26 and down-converter 28 as well as additional components shown in figure 1.

Regarding claims 34, 36 and 37, Fague discloses the radio frequency receiver shown in figure 1. The receiver comprises an analog gain control section for controlling the gain of a received RF signal. The programmable gain amplifiers 23 are controlled by the RSSI circuit 24 (paragraph 0024). The RSSI circuit 24 will recognize the presence

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of a data packet within the RF signal. This packet will be output from the filter 22 and the RSSI circuit will ensure a constant signal is input to the AGC 26. The receiver comprises a digital demodulator 32 for demodulating the output of the gain control section. The demodulator section receives I and Q signals from the downconverter 28. These signals will contain different delays. The receiver comprises a preamble detect circuit 36 that recognizes the presence of a data packet within the received RF signal. The digital demodulator is shown in figure 2. The preamble detect circuit will enable components of the FO determination section 59 of figure 3 (paragraph 0032).

Regarding claim 35, The FIR filters are shown in figure 1.

Regarding claim 38, Fague discloses the radio frequency receiver shown in figure 1. The receiver comprises an analog gain control section for controlling the gain of a received RF signal. The programmable gain amplifiers 23 are controlled by the RSSI circuit 24 (paragraph 0024). The RSSI circuit 24 will recognize the presence of a data packet within the RF signal. This packet will be output from the filter 22 and the RSSI circuit will ensure a constant signal is input to the AGC 26. The receiver comprises a digital demodulator 32 for demodulating the output of the gain control section. The receiver comprises a preamble detect circuit 36 that recognizes the presence of a data packet within the received RF signal. The digital demodulator is shown in figure 2. The preamble detect circuit will enable components of the FO determination section 59 of figure 3 (paragraph 0032). The sample rate is five times the symbol frequency (paragraph 0032). A symbol timing recover (STR) circuit 38 identifies samples of the preamble of the packet and synchronizes the received signal with the

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STR circuit's output (paragraph 0028). The logic state detect block 40 detects the remainder of the data packet (paragraph 0029).

Regarding claim 54, Fague further discloses the sample rate is five times the symbol frequency (paragraph 0032). A symbol timing recover (STR) circuit 38 identifies samples of the preamble of the packet and synchronizes the received signal with the STR circuit's output (paragraph 0028). The logic state detect block 40 detects the remainder of the data packet (paragraph 0029).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Kevin M. Burd 11/17/2007 KEVIN BURD
PRIMARY EXAMINER